CLAIMS:

1. A redundant single event upset suppression system comprising more than one semiconductor register logically connected and including CMOS transistors configured to operate as at least one of a logical cross-coupled Nor Gate SR flip-flop or a logical cross-coupled Nand Gate SR flip-flop, and including inputs that are CMOS gates and insulators, wherein the CMOS gates are back drive resistant thereby isolating external circuitry driving the register.

2. The invention of claim 1 wherein the register operates as a memory.

3. The invention of claim 1 wherein the register can overcome radiation effects.

4. The invention of claim 1 wherein the register is configured as a logical SR latch Flip-flop and its inputs comprise one S and one R input.

5. The invention of claim 1, wherein the inputs drives the gates of the transistors.

6. A redundant single event upset suppression system, comprising:

at least two semiconductor registers logically connected and each including CMOS transistors adapted to operate as a logical cross-coupled Nor Gate SR flip-flop; and

inputs to the register comprised of CMOS gates acting as insulators.

7. The invention of claim 6 wherein the register operates as a memory.

8. The invention of claim 6 wherein the register can overcome radiation effects.

9. The invention of claim 6 wherein the register is configured as a logical SR latch Flip-flop and its inputs comprise one S and one R input.

10. The invention of claim 6, wherein the inputs drives the gates of the transistors.

11. A single event upset suppression system, comprising:

at least two semiconductor registers logically connected and each including CMOS transistors adapted to operate as a logical cross-coupled Nand Gate SR flip-flop; and

inputs to the register comprised of CMOS gates acting as insulators.

12. The invention of claim 11 wherein the register operates as a memory.

13. The invention of claim 11 wherein the register can overcome radiation effects.

14. The invention of claim 11 wherein the register is configured as a logical SR latch Flip-flop and its inputs comprise one S and one R input.

15. The invention of claim 11, wherein the inputs drives the gates of the transistors.